REMARKS

The Examiner's Action mailed on March 18, 2003 has been received and its contents have been carefully considered.

In this Amendment, Applicants have amended claims 1, 3-6 and 8 to define the invention more particularly and distinctly, and added new claims 9-15 to further protect features of the invention disclosed in the application. Claims 1 and 9 are the independent claims. Claims 1-15 are now pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 1-3 have been rejected by the Examiner under 35 U.S.C. §102(b) as being anticipated by *Nakamura* (US Patent No. 5,982,042). It is submitted that these claims patentably distinguish over the cited reference for at least the following reasons.

It is well settled that a reference may anticipate a claim within the purview of 35 U.S.C. §102 only if all the features and all the relationships recited in the claim are taught by the reference either by clear disclosure or under the principle of inherency. However, the cited reference does not disclose, nor does it even suggest, various of the features recited in independent claim 1.

Applicants' amended independent claim 1 recites a bonding pad structure comprising: a first pad for bonding; and at least one second pad for probing, coupled with the first pad, wherein **both of the first pad and the second pad are formed on an IC (Integrated Circuit)**.

In contrast, *Nakamura* discloses a semiconductor wafer including a

semiconductor device, wherein the semiconductor device has a wire-bonding pad 2, formed on the IC 1a; a wafer testing pad, formed on the dicing line 6, which is a cutting region around the IC 1a; and an extension aluminum interconnection 7 electrically connects the wire-bonding pad 2 and the wafer testing pad 3 (Col. 6, line 8–12; FIG. 8). *Nakamura* fails to disclose (or suggest) that both of the first pad and the second pad are formed on the IC; instead, the wafer testing pad revealed by *Nakamura* is formed on the dicing line 6, which is a cutting region around the IC 1a, and removed after wafer testing. As such, it is submitted that claim 1 is not anticipated by (or otherwise rendered obvious by) the cited reference.

Furthermore, it is submitted that claims 2-3 patentably distinguish over the cited reference for at least the same reasons that independent claim 1 is allowable, since claims 2-3 depend from claim 1. It therefore is submitted that the rejection is overcome by the amended claims, and accordingly, should be withdrawn.

Claims 4-8 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura* (US Patent No. 5,982,042) in view of *Kudou et al.* (US Patent No. 6,303,948) and further in view of the remark. It is submitted that these claims patentably distinguish over the applied references.

The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first pad layout and the second pad layout arranged in a linear or staggered manner, as taught by *Kudou et al.*

Kudou et al. discloses a layout for pads and leads for a semiconductor device in order to cope with reductions in chip size, increases in the number of pins of a package, and reductions in the pitch of the pads. *Kudou et al.* lacks any teaching or suggestion

regarding test pads or the arrangement of test pads on an IC. Accordingly, it is submitted that those skilled in the art would not be motivated to arrange the layouts for pads and leads, as taught by *Kudou et al.* in the device of *Nakamura*, except in a hindsight attempt at reconstructing Applicants' claimed invention, or to otherwise combine the teachings of the two references in the manner suggested by the Examiner to overcome the deficiency of *Nakamura*. For at least these reasons, the rejection is respectfully traversed.

In addition, it is submitted that claims 4-8 patentably distinguish over the applied references for at least the same reasons as independent claim 1, from which these claims depend. Therefore, it is respectfully requested that the rejection of claims 4-8 be withdrawn.

Further, it is submitted that new claim 9 patentably distinguishes the invention over the cited references for at least the following additional reason. Applicants' independent claim 9 recites a bonding pad structure comprising: a first pad for bonding; and at least one second pad for probing, coupled with the first pad, wherein **both of the first pad and the second pad are formed on a PCB (printed circuit board)**.

Neither *Nakamura* nor *Kudou et al.* disclose (or suggest) a bonding pad structure in which both of the first pad and the second pad are formed on a PCB (printed circuit board) to avoid probing damage for increasing the yield rate of the PCB products. As such, it is submitted that claim 9 has not been anticipated by (or otherwise rendered obvious by) *Nakamura* and patentably distinguishes over the cited art combination, *Nakamura* in view of *Kudou et al.*

Based on the above, it is submitted that all of the pending claims 1-15 are allowable over the cited references, so that this application is in condition for allowance. Accordingly, notice of allowance and the passing of this case to issue are respectfully requested.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

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Date

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